

MIPI Cable ver. 2.4

for connecting Traced Devices to Fido trace box

DATASHEET

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1. DOCUMENT INFORMATION

1.1. Document history

<i>Version</i>	<i>Date</i>	<i>Comment</i>
1.0	July 01, 2009	First release
1.1	Feb 19, 2010	Legal notices completed
1.2	Mar 12, 2010	Legal notices revised. X4 pin mappings in table 3 fixed

1.2. Terminology and abbreviations

<i>Abbreviation</i>	<i>Description</i>
ESD	Electrostatic Discharge Voltage
JTAG	Joint Test Access Group
LVC MOS	Low Voltage CMOS
LVDS	Low Voltage differential signalling
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PTI	MIPI Parallel Trace Interface

1.3. References

- [1] MIPI Alliance Standard for Test & Debug – Parallel Trace Interface.
 [2] MIPI Alliance Recommendation for Test & Debug – Parallel Trace and Debug Connector, version 1.0.

2. OVERVIEW

The MIPI Cable v2.4 is designed to connect any traced device providing MIPI Alliance recommended 34-pin Basic Debug connector [2] to Fido trace box.

Additionally, the cable provides 34-pin and 20-pin JTAG extender connectors for simultaneous attaching of JTAG debuggers.

The traced device connector provides two exclusively independent logical groups of signals – the Parallel Trace Interface (PTI interface) signals and the JTAG Debug Interface signals.

The MIPI Cable v2.4 feeds the Trace Interface signals to Fido trace box. To transfer over significantly long cable, the trace signals are on the cable PCB converted beforehand from the LVCMOS levels to the LVDS signals.

The JTAG Debug Interface signals including their independent reference voltage provided by traced device are fed directly to the JTAG connectors. No any electronic circuitry is attached to those signals.

Note that none of the Trace Interface signals is fed to the cable JTAG connectors and none of the JTAG Debug Interface signals is fed to Fido trace box.

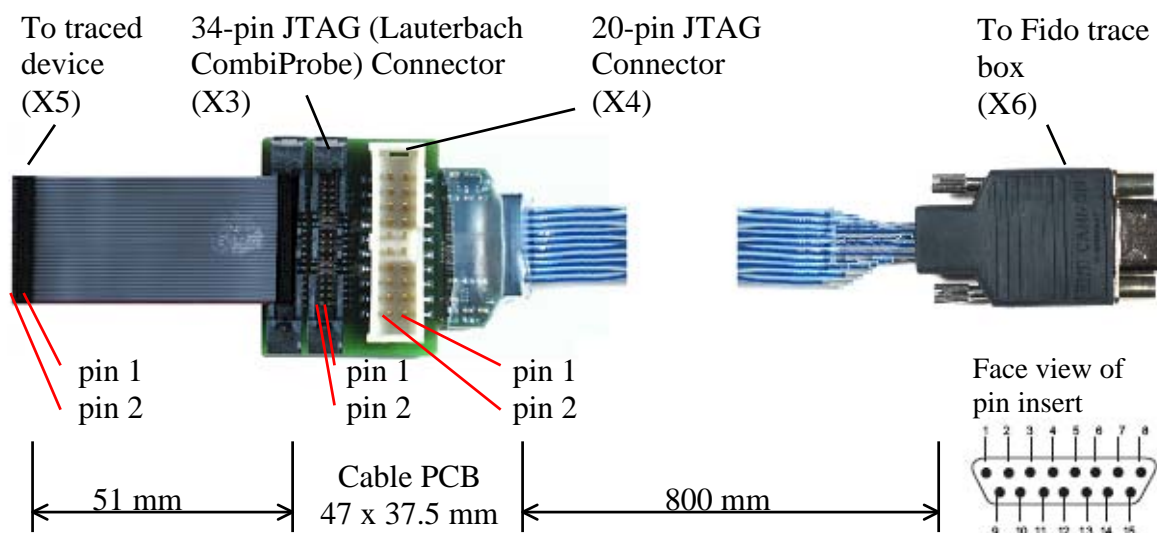


Figure 1. MIPI Cable v2.4 overview

The cable logical structure and connections are presented on Figure 2.

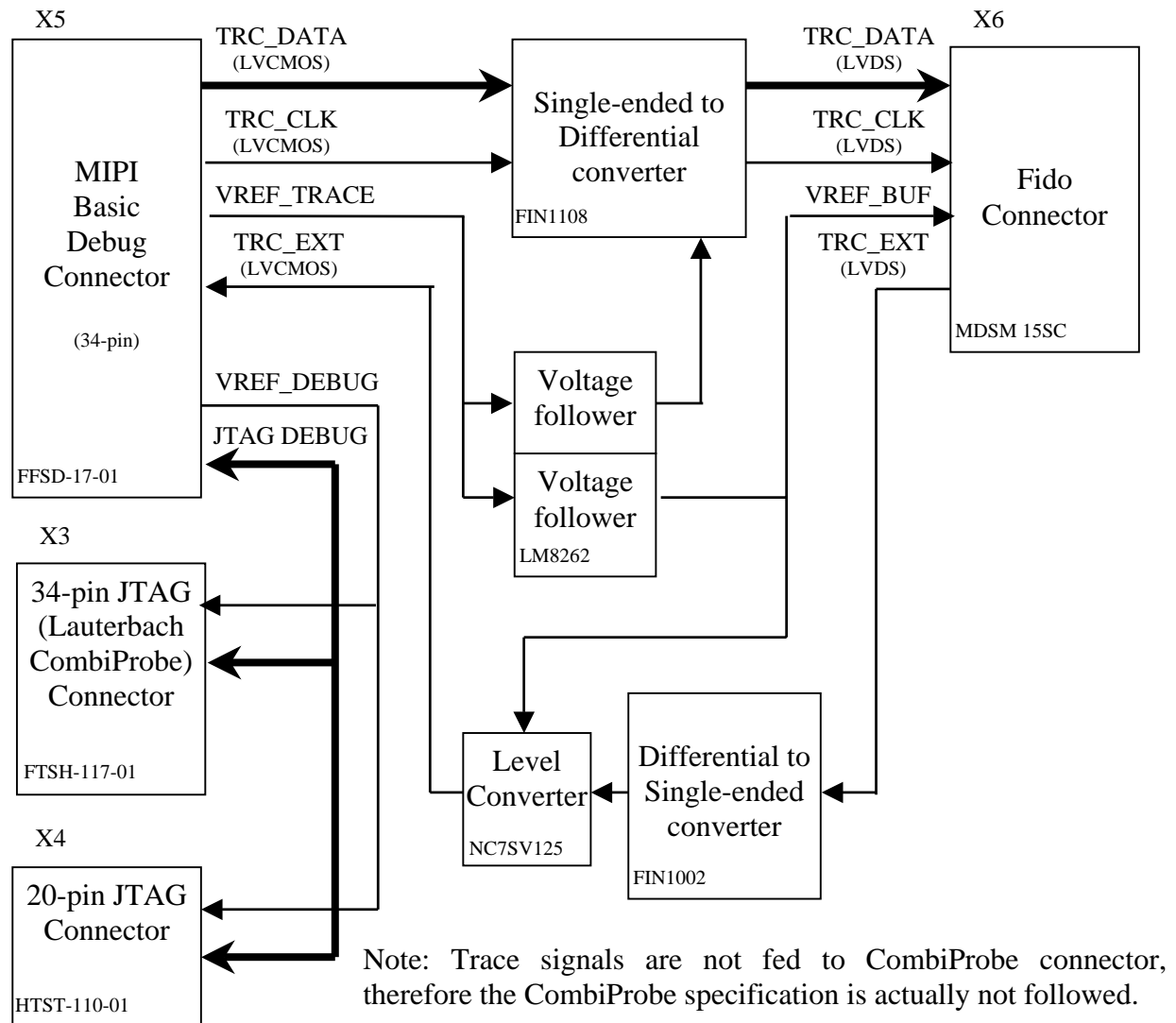


Figure 2. MIPI Cable v2.4 functional description

3. CABLE CONNECTORS

MIPI Cable v2.4 provides the following connectors:

- MIPI Basic Debug Connector for attaching to traced device. Samtec part FFSD-17-01. For pin mappings, see Table 1.
- 34-pin JTAG (Lauterbach CombiProbe) Connector for simultaneous attaching of JTAG debuggers to traced device. All JTAG DEBUG interface signals from MIPI Basic Debug Connector are routed directly to this connector. Note that the Trace Interface signals are actually not fed to this connector and therefore the simultaneous tracing with Lauterbach CombiProbe is not supported. Samtec part FTSH-117-01-F-DV-EJ-K-P. For pin mappings, see Table 2.
- 20-pin JTAG Connector for attaching JTAG debuggers. All the JTAG DEBUG interface signals from MIPI Basic Debug Connector are routed directly to this connector. Samtec part HTST-110-01. For pin mappings, see Table 3.
- Fido box connector. All Trace Interface signals from MIPI Basic Debug Connector are routed to this connector. ITT Cannon part MDSM 15SC. For pin mappings, see Table 4.

Table 1. MIPI Basic Debug Connector (X5)

<i>Pin</i>	<i>Direction</i>	<i>Symbol</i>	<i>Description</i>
1		VREF_DEBUG	JTAG Debug Interface Reference Voltage, to JTAG connectors
2		JTAG TMS	to JTAG connectors
3		GND	Ground (0V)
4		JTAG TCK	to JTAG connectors
5		GND	Ground (0V)
6		JTAG TDO	to JTAG connectors
7		NC	Not connected
8		JTAG TDI	to JTAG connectors
9		NC	Not connected
10		nReset	to JTAG connectors
11		GND	Ground (0V)
12		RTCK	to JTAG connectors
13		GND	Ground (0V)
14		BCE	to JTAG connectors
15		GND	Ground (0V)
16		NTRST	to JTAG connectors
17		GND	Ground (0V)
18		TRIGIN	to JTAG connectors
19		GND	Ground (0V)
20		TRIGOUT	to JTAG connectors
21		GND	Ground (0V)
22	Input	TRC_CLK	Trace clock, to Fido connector
23		GND	Ground (0V)
24	Input	TRC_DATA0	Trace Data bit 0, to Fido connector
25		GND	Ground (0V)
26	Input	TRC_DATA1	Trace Data bit 1, to Fido connector

<i>Pin</i>	<i>Direction</i>	<i>Symbol</i>	<i>Description</i>
27		GND	Ground (0V)
28	Input	TRC_DATA2	Trace Data bit 2, to Fido connector
29		GND	Ground (0V)
30	Input	TRC_DATA3	Trace Data bit 3, to Fido connector
31		GND	Ground (0V)
32	Output	TRC_EXT	Return channel, to Fido connector
33		GND	Ground (0V)
34	Input	VREF_TRACE	Trace Interface Reference voltage, to Fido connector through voltage follower.

Table 2. 34-pin JTAG (Lauterbach CombiProbe) Connector (X3)

<i>Pin</i>	<i>Symbol</i>	<i>Description</i>
1	VREF_DEBUG	JTAG Debug Interface Reference Voltage. See Table 1.
2	JTAG TMS	See Table 1.
3	GND	See Table 1.
4	JTAG TCK	See Table 1.
5	GND	Ground (0V)
6	JTAG TDO	See Table 1.
7	NC	Not connected
8	JTAG TDI	See Table 1.
9	NC	Not connected
10	nReset	See Table 1.
11	GND	Ground (0V)
12	RTCK	See Table 1.
13	GND	Ground (0V)
14	BCE	See Table 1.
15	GND	Ground (0V)
16	NTRST	See Table 1.
17	GND	Ground (0V)
18	TRIGIN	See Table 1.
19	GND	Ground (0V)
20	TRIGOUT	See Table 1.
21	GND	Ground (0V)
22		
23	GND	Ground (0V)
24		
25	GND	Ground (0V)
26		
27	GND	Ground (0V)
28		
29	GND	Ground (0V)
30		
31	GND	Ground (0V)
32		
33	GND	Ground (0V)
34		

Table 3. 20-pin JTAG Connector (X4)

NB! Pin mapping follows legacy ARM 20-pin header mapping.

<i>Pin</i>	<i>Symbol</i>	<i>Description</i>
1	VREF_DEBUG	JTAG Debug Interface Reference Voltage. See Table 1.
2	-	Not connected
3	NTRST	See Table 1.
4	GND	Ground (0V)
5	JTAG TDI	See Table 1.
6	GND	Ground (0V)
7	JTAG TMS	See Table 1.
8	GND	Ground (0V)
9	JTAG TCK	See Table 1.
10	GND	Ground (0V)
11	RTCK	See Table 1.
12	GND	Ground (0V)
13	JTAG TDO	See Table 1.
14	GND	Ground (0V)
15	nReset	See Table 1.
16	GND	Ground (0V)
17	TRIGIN	See Table 1.
18	GND	Ground (0V)
19	TRIGOUT	See Table 1.
20	GND	Ground (0V)

Table 4. Fido Connector (X6)

<i>Pin</i>	<i>Direction</i>	<i>Level</i>	<i>Symbol</i>	<i>Description</i>	<i>Respective signal in MIPI Basic Debug Connector (Table 1)</i>
1	Output	LVDS	TRC_CLK_P	Trace clock, positive	TRC_CLK
2	Output	LVDS	TRC_CLK_N	Trace clock, negative	
3	Output	LVDS	TRC_D0_P	Trace data, bit 0, positive	TRC_DATA0
4	Output	LVDS	TRC_D0_N	Trace data, bit 0, negative	
5	Output	LVDS	TRC_D1_P	Trace data, bit 1, positive	TRC_DATA1
6	Output	LVDS	TRC_D1_N	Trace data, bit 1, negative	
7	Output	LVDS	TRC_D2_P	Trace data, bit 2, positive	TRC_DATA2
8	Output	LVDS	TRC_D2_N	Trace data, bit 2, negative	
9	Input	DC	VCC	+3.3V cable supply voltage	
10	Output	DC	VREF_BUF	Buffered Trace Reference voltage	VREF_TRACE
11	Input	LVDS	TRC_Q_P	Return channel, positive	TRC_EXT
12	Input	LVDS	TRC_Q_N	Return channel, negative	
13	Output	LVDS	TRC_D3_P	Trace data, bit 3, positive	TRC_DATA2
14	Output	LVDS	TRC_D3_N	Trace data, bit 3, negative	
15		DC	GND	Ground	GND

4. ELECTRICAL CHARACTERISTICS

The absolute maximum ratings are presented in Table 5. They are stress ratings only and the device functional operation at these or any other conditions beyond those listed in Table 6 is not implied. Stresses beyond those listed in Table 5 might cause permanent damage to the device. Exposure to the absolute maximum ratings conditions for extended periods of time might affect the device reliability. All the voltages in Table 5 and Table 6 are relative to the MIPI Cable ground voltage.

Table 5. Absolute maximum ratings

<i>Description</i>	<i>Min</i>	<i>Max</i>
Input voltage, Trace Interface signals	-0.5 V	+4.6 V
Input voltage, VREF_TRACE	-1.6 V	+10 V
ESD, Human body model	-	+/-7500 V
ESD, Machine model	-	+/-400 V
Storage temperature	-65 °C	+150 °C

Table 6. DC characteristics

<i>Description</i>	<i>Con- nector</i>	<i>Symbol</i>	<i>Unit</i>	<i>Min</i>	<i>Max</i>
Input voltage, VREF_TRACE	X5 (X1)	Vref	V	1.1	3.3
Input voltage, Trace signals, Low		Vil	V	0	Vref/2-0.3
Input voltage, Trace signals, High		Vih	V	Vref/2+0.3	3.3
Input resistance, VREF_TRACE		Rrefi	KOhm	90	
Input current, Trace signals		Iin	µA		±20
Input capacitance, Trace signals		Cin	pF		10
Output voltage, TRC_EXT, Low (Note 1)			Vol	V	0
Output voltage, TRC_EXT, High (Note 2)		Voh	V	0.74*Vref	1.02*Vref
Output differential voltage, Trace signals	X6	Vod	mV	250	450
Output short circuit current, VREF_BUF		Irefs	mA	20	
Supply voltage VCC		Vcc	V	3.0	3.6
Operation temperature	-	T	°C	-40	+75

Note 1. Output current, TRC_EXT, Low:

I_{ol} = 2 mA @ VREF_TRACE = 1.1...1.3 V;

I_{ol} = 4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = 6 mA @ VREF_TRACE = 1.65...2.7 V;

I_{ol} = 12 mA @ VREF_TRACE = >2.7 V.

Note 2. Output current, TRC_EXT, High:

I_{ol} = -2 mA @ VREF_TRACE = 1.1...1.3 V;

I_{ol} = -4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = -6 mA @ VREF_TRACE = 1.65...2.7 V;

I_{ol} = -12 mA @ VREF_TRACE = >2.7 V.

5. SCHEMATICS

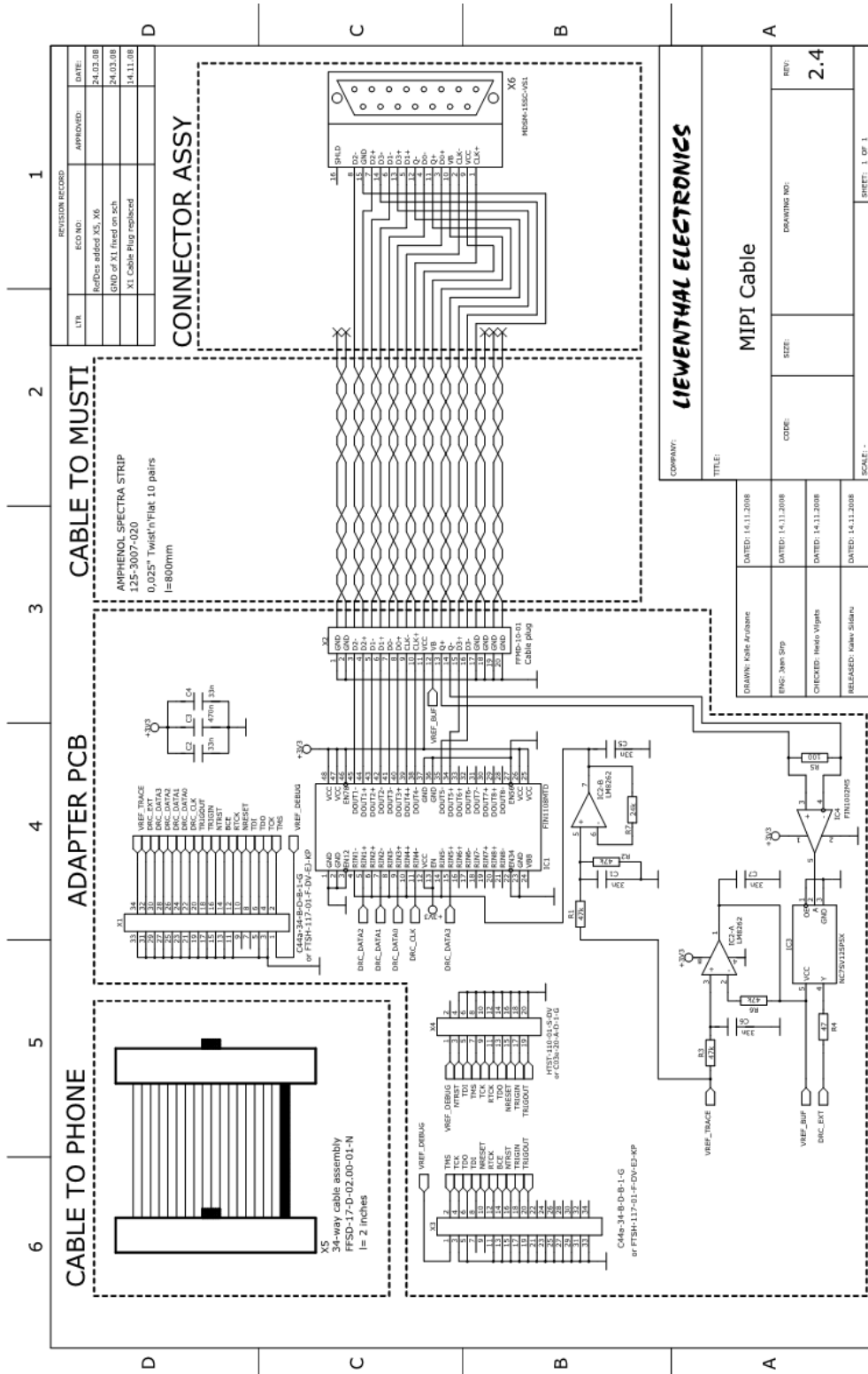


Figure 3. MIPI Cable 2.4 schematics