

MIPI 60pin QTH Trace Cable ver. 1.2

For connecting traced devices to Fido trace box

preliminary
DATASHEET

Version 1.2, 07 Jun 2010

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1. DOCUMENT INFORMATION

1.1. Document history

<i>Version</i>	<i>Date</i>	<i>Comment</i>
1.0	May 05, 2010	First draft release
1.1	May 11, 2010	Fixed some typos. VrefDebug and VrefTrace min/max values updated.
1.2	June 07, 2010	Cable connector dimensions added. Document updated.

1.2. Terminology and abbreviations

<i>Abbreviation</i>	<i>Description</i>
ESD	Electrostatic Discharge Voltage
FPGA	Field-Programmable Gate Array
JTAG	Joint Test Access Group
LVC MOS	Low Voltage CMOS
LVDS	Low Voltage differential signalling
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PTI	MIPI Parallel Trace Interface
STP	System Trace Protocol

1.3. References

[1] MIPI Alliance Standard for Test & Debug – Parallel Trace Interface.

[2] MIPI Alliance Recommendation for Test & Debug – Parallel Trace and Debug Connector, version 1.0.

2. OVERVIEW

The MIPI 60 Pin Cable is designed for tracing devices providing MIPI Alliance recommended Samtec QSH 60 pin connector with Fido and Musti trace boxes. See Figure 1.

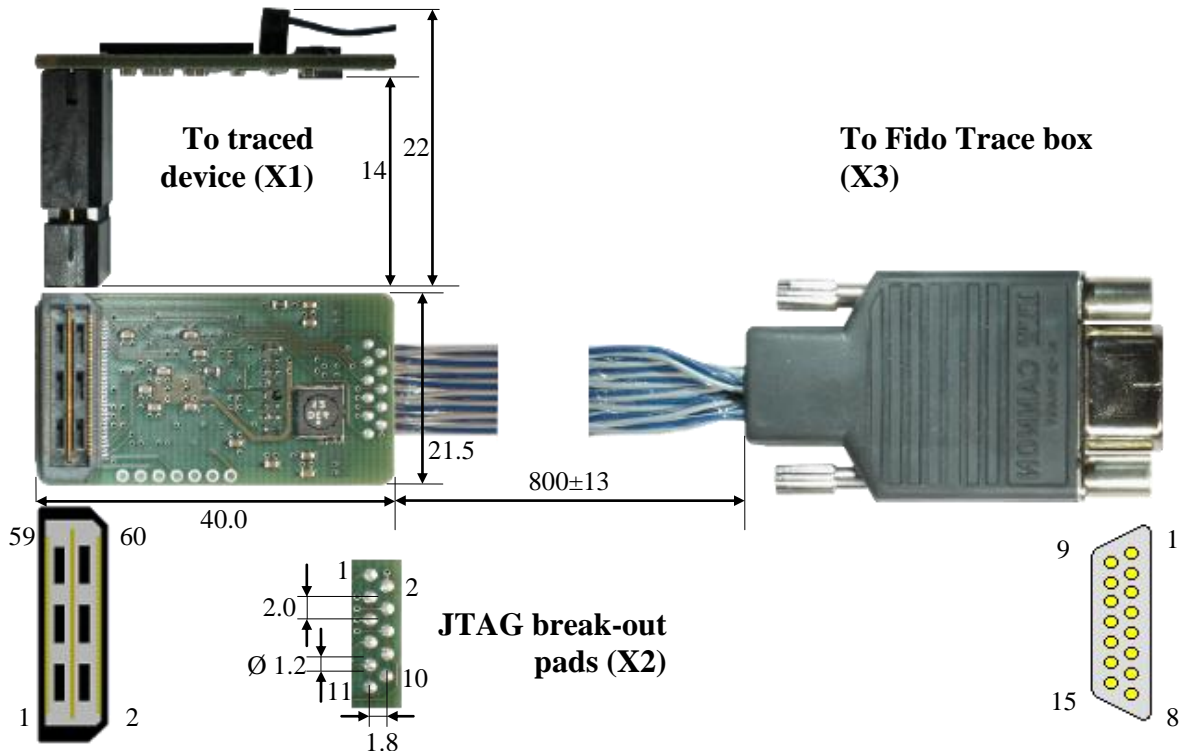


Figure 1. MIPI 60 Pin Cable

Actually, the cable can be considered as an (re)programmable FPGA-based device (see Figure 2). The trace box initializes cable FPGA with software at run time respective to selected trace protocol. The actual meaning and usage of trace signals depends on the software loaded into the FPGA. Currently, the implemented software supports two STP protocols: the muxed STP and the dedicated STP (see Supported trace protocols).

For attaching external JTAG debuggers, the cable provides optional JTAG break-out pads (X2) that are connected directly to JTAG signals in target connector (X1).

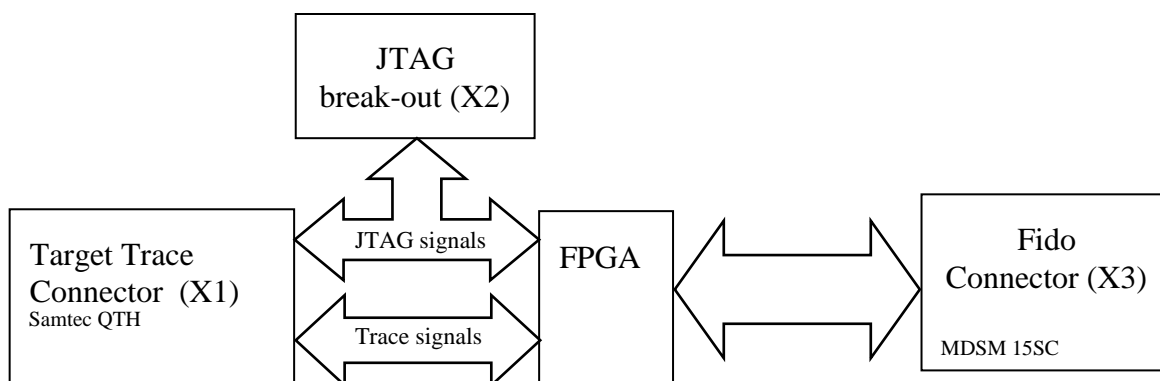


Figure 2: MIPI 60 Pin Cable functional description

3. CABLE CONNECTORS

MIPI 60 Pin Cable provides the following connectors:

- Trace Connector (X1). Samtec QTH-030-04-L-D-A. For pin mappings, see Table 1.
- JTAG break-out pads (X2).
- Fido box connector (X3). ITT Cannon part MDSM 15SC. For pin mappings, see Table 3.

Table 1. Trace Connector (X1)

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
VREF_DEBUG	1	2	TMS/TMSC
TCK/ TCKC	3	4	TDO
TDI	5	6	nRESET
RTCK	7	8	TRST_PD
nTRST	9	10	TRIGIN
TRIGOUT	11	12	VREF_TRACE2
TRC_CLK[0]	13	14	NC
Target Presence Detect	15	16	GND
TRC_DATA[0][0]/TRC_CTRL	17	18	NC
TRC_DATA[0][1]	19	20	NC
TRC_DATA[0][2]	21	22	NC
TRC_DATA[0][3]	23	24	NC
TRC_DATA[0][4]	25	26	NC
TRC_DATA[0][5]	27	28	NC
TRC_DATA[0][6]	29	30	NC

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
TRC_DATA[0][7]	31	32	NC
TRC_DATA[0][8]	33	34	NC
NC	35	36	NC
NC	37	38	TRC_DATA[2][0]
NC	39	40	TRC_DATA[2][1]
NC	41	42	TRC_DATA[2][2]
NC	43	44	TRC_DATA[2][3]
NC	45	46	NC
NC	47	48	NC
NC	49	50	NC
NC	51	52	NC
NC	53	54	UART[2]
NC	55	56	UART[0]
GND	57	58	GND
NC	59	60	TRC_CLK[2]

Table 2. JTAG break-out pads (X2)

<i>Pin</i>	<i>Symbol</i>	<i>Comment</i>
1	nRESET	Connected to pin 6 in Trace Connector X1
2	GND	
3	nTRST	Connected to pin 9 in Trace Connector X1
4	TDI	Connected to pin 5 in Trace Connector X1
5	TMS/TMSC	Connected to pin 2 in Trace Connector X1
6	VREF_DEBUG	Connected to pin 1 in Trace Connector X1
7	TDO	Connected to pin 4 in Trace Connector X1
8	TCK/ TCKC	Connected to pin 3 in Trace Connector X1
9	RTCK	Connected to pin 7 in Trace Connector X1
10	NC	
11	NC	

Table 3. Fido Connector (X3)

<i>Pin</i>	<i>Direction</i>	<i>Level</i>	<i>Symbol</i>	<i>Description</i>
1	Output	LVDS	CLK_P	Clock, positive
2	Output	LVDS	CLK_N	Clock, negative

<i>Pin</i>	<i>Direction</i>	<i>Level</i>	<i>Symbol</i>	<i>Description</i>
3	Output	LVDS	D0_P	Data to trace box, bit 0, positive
4	Output	LVDS	D0_N	Data to trace box, bit 0, negative
5	Output	LVDS	D1_P	Data to trace box, bit 1, positive
6	Output	LVDS	D1_N	Data to trace box, bit 1, negative
7	Output	LVDS	D2_P	Data to trace box, bit 2, positive
8	Output	LVDS	D2_N	Data to trace box, bit 2, negative
9	Input	DC	VCC	+3.3V cable supply voltage
10	Output	DC	VREF_BUF	Buffered Trace Reference voltage
11	Input	LVDS	Q_P	Data from trace box, positive
12	Input	LVDS	Q_N	Data from trace box, negative
13	Output	LVDS	D3_P	Data to trace box, bit 3, positive
14	Output	LVDS	D3_N	Data to trace box, bit 3, negative
15		DC	GND	Ground

4. SUPPORTED TRACE PROTOCOLS

Currently the cable software supports only 4-bit STP in two variants – muxed and dedicated STP. Only one STP variant can be selected (by trace box) at a time. The actual trace signals used in these modes are described in tables Table 4 and Table 5. The rest signals routed from connector X1 pins to FPGA pins are left floating in FPGA image.

FPGA image captures STP nibbles (actually PTI nibbles) and forwards these to trace box for additional (post)processing.

STP signals DC characteristics depend on actual FPGA image loaded into cable FPGA at run time and depend therefore on actual software controlling the cable. Refer to software documentation for details.

From cable hardware viewpoint, it must be possible to support at least 100MHz TRC_CLK frequency.

Table 4: Trace Connector (X1) pins usage in case of muxed STP

<i>Pin</i>	<i>Signal</i>	<i>Direction</i>	<i>Description</i>
1	VREF_DEBUG	input	Reference voltage for UART[0].
12	VREF_TRACE2	input	Reference voltage for TRC_DATA and TRC_CLK signals.
13	TRC_CLK[0]	input	STP clock
19	TRC_DATA[0][1]	input	STP data, bit 0
21	TRC_DATA[0][2]	input	STP data, bit 1
23	TRC_DATA[0][3]	input	STP data, bit 2
25	TRC_DATA[0][4]	input	STP data, bit 3
56	UART[0]	output	Return data (to traced device)

Table 5: Trace Connector (X1) pins usage in case of dedicated STP

<i>Pin</i>	<i>Signal</i>	<i>Direction</i>	<i>Description</i>
1	VREF_DEBUG	input	Reference voltage for UART[2].
12	VREF_TRACE2	input	Reference voltage for TRC_DATA and TRC_CLK signals.
38	TRC_DATA[2][0]	input	STP data, bit 0
40	TRC_DATA[2][1]	input	STP data, bit 1
42	TRC_DATA[2][2]	input	STP data, bit 2
44	TRC_DATA[2][3]	input	STP data, bit 3
54	UART[2]	output	Return data (to traced device)
60	TRC_CLK[2]	input	STP clock

5. ELECTRICAL CHARACTERISTICS

The absolute maximum ratings are presented in Table 6. They are stress ratings only and the device functional operation at these or any other conditions beyond those listed in Table 7 are not implied. Stresses beyond those listed in Table 6 might cause permanent damage to the device. Exposure to the absolute maximum ratings conditions for extended periods of time might affect the device reliability. All the voltages in Table 6 and Table 7 are relative to the MIPI Cable ground voltage.

Table 6: Absolute maximum ratings

<i>Description</i>	<i>Min</i>	<i>Max</i>
Input voltage, Trace Interface signals	-0.5 V	+4.6 V
Input voltage, VREF_TRACE	-0.5 V	+4.6 V
Input voltage, VREF_DEBUG	-0.5 V	+4.6 V
ESD, Human body model	-	+/-2000 V
ESD, Machine model	-	+/-200 V
Storage temperature	-65 °C	+150 °C

Table 7: DC characteristics

<i>Description</i>	<i>Conn.</i>	<i>Symbol</i>	<i>Unit</i>	<i>Min</i>	<i>Max</i>
Input voltage, VREF_TRACE	X1	VrefT	V	0.8	3.6
Input voltage, VREF_DEBUG		VrefD	V	1.1	3.0
Input voltage, Trace signals, Low		Vil	V	0	VrefT/2-0.3

<i>Description</i>	<i>Conn.</i>	<i>Symbol</i>	<i>Unit</i>	<i>Min</i>	<i>Max</i>
Input voltage, Trace signals, High		V _{ih}	V	V _{refT} /2+0.2	3.6
Input voltage, Trace signals, Low		V _{il}	V	0	V _{refT} /2-0.2
Input current, Trace signals		I _{in}	μA		±10
Input capacitance, Trace signals		C _{in}	pF		10
Output voltage, UART, Low (Note 1)		V _{ol}	V	0	0.4
Output voltage, UART, High (Note 2)		V _{oh}	V	V _{refD} -0.4	V _{refD}
Output differential voltage, Trace signals		V _{od}	mV	250	450
Output short circuit current, VREF_BUF	X3	I _{refs}	mA	20	
Supply voltage VCC		V _{cc}	V	3.15	3.6
Operation temperature		-	T	°C	-40

Note 1. Output current, UART, Low:

I_{ol} = 2 mA @ VREF_TRACE = 1.2...1.3 V;

I_{ol} = 4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = 6 mA @ VREF_TRACE = 1.7...2.5 V.

Note 2. Output current, UART, High:

I_{ol} = -2 mA @ VREF_TRACE = 1.2...1.3 V;

I_{ol} = -4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = -6 mA @ VREF_TRACE = 1.7...2.5 V.