

Fido Interface Electrical Specification

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1. Basic information

1.1. Document history

<i>Version</i>	<i>Date</i>	<i>Comment</i>
1.0	07.05.2009	First edition
1.1	19.06.2009	Fido software version updated
1.2	22.06.2009	Comment in Table 1 changed
1.3	19.02.2010	Legal notices completed
1.4	12.03.2010	Legal notices revised

1.2. Terminology and abbreviations

<i>Abbreviation</i>	<i>Description</i>
FPGA	Field Programmable Gate Array
PTI	MIPI standardized Parallel Trace Interface
TS	Target System (the system being debugged)

1.3. References

[1] MIPI Alliance Standard for Test & Debug – Parallel Trace Interface, draft ver.0.9, 05. June 2006; MIPI Alliance, Inc.

[2] MIPI Alliance Recommendation for Test & Debug – Parallel Trace and Debug Connector, version 1.0.

2. Introduction

Fido trace interface bases on Parallel Trace Interface (PTI) that is described in details in [1].

Fido current version supports the 4-bit PTI (i.e. four data signals TRC_DATA[3:0]) with PTI clock signal (TRC_CLK) sourced by Target System (TS). TRC_CLK fronts are expected to be aligned to the centre of TRC_DATA valid window.

Fido trace interface is formed from several components, each influencing on the actual values of interface characteristics. The Fido system components affecting the interface characteristics are:

- Cable connecting the Fido box to TS.
- FPGA image loaded into Fido box at runtime.

This document presents the PTI specifications of system including Fido software version 1.3.x.x, MIPI Cable version 2.4 and Fido box version 2.3.

3. Pin Mapping

For connecting to TS the MIPI cable version 2.4 has the MIPI recommended 34-pin header.

Table 1. Fido trace interface (MIPI cable ver. 2.4) header pin mappings.

<i>Signal</i>	<i>Pin#</i>	<i>Pin#</i>	<i>Signal</i>	<i>Comment</i>
VREF_DEBUG	1	2	JTAG TMS	These pins and pin 1 are feed directly to 20-pin and 34-pin JTAG Connector, both placed near the cable header on cable PCB. Characteristics of those signals are not the subject of Fido specification and are determined by devices attached to respective connectors.
GND	3	4	JTAG TCK	
GND	5	6	JTAG TDO	
NC	7	8	JTAG TDI	
NC	9	10	nRESET	
GND	11	12	RTCK	
GND	13	14	BCE	
GND	15	16	nTRST	
GND	17	18	TRIGIN	
GND	19	20	TRIGOUT	
GND	21	22	TRC_CLK	PTI trace clock pin
GND	23	24	TRC_DATA[0]	PTI trace data pins
GND	25	26	TRC_DATA[1]	
GND	27	28	TRC_DATA[2]	
GND	29	30	TRC_DATA[3]	
GND	31	32	TRC_EXT	Generic trace sideband output (used for sending data to TS)
GND	33	34	VREF_TRACE	Trace interface reference voltage

4. Absolute Maximum Ratings

Fido trace interface Absolute Maximum Ratings are determined only by the cable connecting the TS and Fido box, i.e. by the MIPI version 2.4 34-pin cable.

Absolute maximum ratings (see Table 2) are stress ratings only, and the functional operation of device at these or any other conditions beyond those listed in Table 3 is not implied. Stresses beyond those listed in Table 2 might cause permanent damage to the device. Exposure to the Absolute Maximum Ratings conditions for long periods might affect on the device reliability.

All voltages in Table 2 are relative to Ground voltage of the MIPI Cable.

Table 2. Fido trace interface Absolute Maximum Ratings with MIPI Cable v.2.4.

<i>Description</i>	<i>Min</i>	<i>Max</i>
Input voltage, TRC Interface	-0.5 V	+4.6 V
Input voltage, VREF_TRACE	-1.6 V	+10 V
ESD, Human body model	-	+/-7500 V
ESD, Machine model	-	+/-400 V

5. DC Specifications

Fido trace interface DC characteristics are presented in Table 3. All the voltages are relative to the MIPI Cable ground voltage.

Table 3. Fido trace interface DC specifications with MIPI Cable v.2.4

<i>Description</i>	<i>Symbol</i>	<i>Unit</i>	<i>Min</i>	<i>Max</i>
Input voltage, VREF_TRACE	Vref	V	1.1	3.3
Input voltage, TRC_DATA and TRC_CLK signals, Low	Vil	V	0	Vref/2-0.3
Input voltage, TRC_DATA and TRC_CLK signals, High	Vih	V	Vref/2+0.3	3.3
Input resistance, VREF_TRACE	Rrefi	KOhm	90	
Input current, TRC_DATA and TRC_CLK signals	Iin	μA		±20
Input capacitance, TRC_DATA and TRC_CLK signals	Cin	pF		10
Output voltage, TRC_EXT, Low (Note 1)	Vol	V	0	0.26*Vref
Output voltage, TRC_EXT, High (Note 2)	Voh	V	0.74*Vref	1.02*Vref
Operation temperature	T	°C	-40	+75

Note 1. Output current, TRC_EXT, Low:

I_{ol} = 2 mA @ VREF_TRACE = 1.1...1.3 V;

I_{ol} = 4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = 6 mA @ VREF_TRACE = 1.65...2.7 V;

I_{ol} = 12 mA @ VREF_TRACE = >2.7 V.

Note 2. Output current, TRC_EXT, High:

I_{ol} = -2 mA @ VREF_TRACE = 1.1...1.3 V;

I_{ol} = -4 mA @ VREF_TRACE = 1.4...1.6 V;

I_{ol} = -6 mA @ VREF_TRACE = 1.65...2.7 V;

I_{ol} = -12 mA @ VREF_TRACE = >2.7 V.

6. AC Specifications

Fido trace interface AC characteristics are depending mainly on the FPGA image loaded into Fido box. These characteristics are in continuous improvement – in the next Fido software releases, for example, the *autofocus* feature will be implemented. The task of autofocus is to adjust the PTI TRC_DATA signal delays in Fido automatically and thus capture the data at the centre of Trace Data Valid Window.

Table 4 presents the PTI AC specifications for system consisting of Fido software version 1.3.x.x, MIPI cable version 2.4 and Fido box version 2.3.

Table 4. Fido trace interface AC specifications.

	<i>Symbol</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
TRC_DATA setup time	Tds	2.5		ns
TRC_DATA hold time	Tdh	1.0		ns
TRC_CLK frequency	Fclk	0.001	99	MHz

